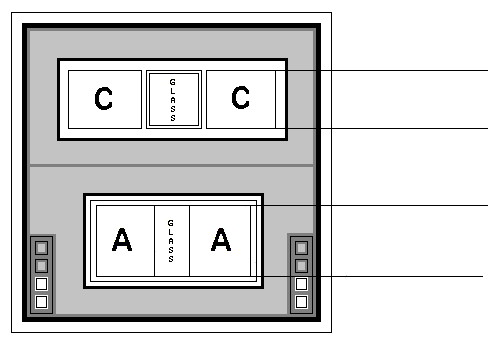
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.022”**

**.022”**



**0.0045”**

**0.004”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” Min.**

**Backside Potential: ISOLATED**

**Mask Ref: ZHR**

**APPROVED BY: DK DIE SIZE .022” X .022” DATE: 8/26/21**

**MFG: ALLEGRO / SPRAGUE THICKNESS .010” P/N: 1N4568A**

**DG 10.1.2**

#### Rev B, 7/1